



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
[www.uspto.gov](http://www.uspto.gov)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/768,185	02/02/2004	Toshio Ito	OKI.639	3670
20987	7590	06/15/2005	EXAMINER	
VOLENTINE FRANCOS, & WHITT PLLC ONE FREEDOM SQUARE 11951 FREEDOM DRIVE SUITE 1260 RESTON, VA 20190				GEBREMARIAM, SAMUEL A
ART UNIT		PAPER NUMBER		
		2811		

DATE MAILED: 06/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>
	10/768,185	ITO, TOSHIO
	Examiner Samuel A. Gebremariam	Art Unit 2811

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) Responsive to communication(s) filed on 28 March 2005.
- 2a) This action is **FINAL**.                    2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) Claim(s) 1-4, 6-11, 13, 14 and 16-20 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) Claim(s) \_\_\_\_\_ is/are allowed.
- 6) Claim(s) 1-3, 6-11, 13, 14 and 16-20 is/are rejected.
- 7) Claim(s) 4 is/are objected to.
- 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on \_\_\_\_\_ is/are: a) accepted or b) objected to by the Examiner.  
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
 a) All    b) Some \* c) None of:  
 1. Certified copies of the priority documents have been received.  
 2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s)/Mail Date. _____
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)
3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____	6) <input type="checkbox"/> Other: _____

## DETAILED ACTION

### ***Claim Rejections - 35 USC § 103***

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1-3, 6-11, and 13-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ochiai in view of Basceri et al. US patent No. 6,444,478.

Regarding claim 1, Ochiai teaches (fig. 3) a ferroelectric capacitor comprising: a bottom electrode (24) which has a first region (end portion of 23) and a second region (21), wherein the first region has a first thickness and the second region has a second thickness greater than the first thickness (refer to fig. 3) and wherein the second region is arranged at a central area of the bottom electrode (refer to fig. 3) and the first region is arranged at a peripheral area of the bottom electrode (fig. 3), a ferroelectric layer formed on the second region of the bottom electrode (24), and a top electrode (26) formed on the ferroelectric layer formed on the middle portion of the lower electrode and also covering lower electrode at the periphery), and wherein a side surface of the first region of the bottom electrode, a side surface of the ferroelectric layer and a side surface of the top electrode are aligned (refer to fig. 3).

Ochiai does not teach a dielectric layer formed on the first region of the bottom electrode wherein the dielectric layer is sandwiched between the first region of the bottom electrode and the ferroelectric layer.

Basceri teaches (fig. 1) the process of forming dielectric layer (12) comprising two dielectric layers (14) and (16).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the dual dielectric layer taught by Basceri in the structure of Ochiai in order to form high capacitance memory device.

The combined structure of Ochiai and Basceri provides a dielectric layer that is sandwiched between the first region of the bottom electrode and the ferroelectric layer.

Furthermore the combined structure of Ochiai and Basceri would have a side surface of the first region of the bottom electrode, a side surface of the dielectric layer, a side surface of the ferroelectric layer and a side surface of the top electrode that are aligned.

Regarding claim 2, Ochiai teaches substantially the entire claimed structure of claim 1 above including the ferroelectric layer includes a damaged area, which is formed on the dielectric layer. Ochiai teaches patterned layers (fig. 3) where the sides of the layers that are aligned. APA teaches (page 2) that etching of the bottom electrode, ferroelectric layer and the top electrode would cause damage on the ferroelectric dielectric layer. Therefore Ochiai inherently teaches a damaged ferroelectric layer.

Regarding claim 3, Ochiai teaches substantially the entire claimed structure of claim 1 above including the bottom electrode (23) comprises the first region and the second as a single unitary electrode (refer to fig. 3).

Regarding claim 6, Ochiai teaches substantially the entire claimed structure of claim 1 above including the bottom electrode and the top electrode are made of an

oxidation resistance metal or a conductive metal oxide (col. 6, lines 14-15 and col. 9, lines 14-26).

Regarding claim 7, Ochiai teaches substantially the entire claimed structure of claim 8 above including the upper layer of the second region (21) of the bottom electrode (24) is made of a material different than the first region (23) and the lower layer of the second region of the bottom electrode (lower layer of 21).

Regarding claim 8, Ochiai teaches substantially the entire claimed structure of claim 1 above including the second region of the bottom electrode includes a lower layer (21) and an upper layer (23).

Regarding claim 9, Ochiai teaches substantially the entire claimed structure of claims 1 and 7 above including the upper layer of the second region of the bottom electrode is made of platinum (col. 11, lines 1-3).

Regarding claims 10 and 13, Ochiai teaches (fig. 3) substantially the entire claimed structure of claim 1 above including a ferroelectric capacitor comprising: a bottom electrode having a step area (24); a top electrode (26); a ferroelectric layer (23) formed between the bottom electrode and the top electrode; and a dielectric spacer (combination of Ochiai and Basceri) formed between the bottom electrode (32) and the top electrode (36), wherein a distance between the bottom electrode (24) and the top electrode (26) at the step area (end portion of 24) is greater than a distance between the bottom electrode and the top electrode at a central area (central portion of 24) of the ferroelectric capacitor and wherein the dielectric spacer decreases an electric field strength at a peripheral area of the capacitor (refer to fig. 3).

Regarding claim 11, Ochiai teaches substantially the entire claimed structure of claim 1 above including the bottom electrode (24) includes a projecting portion (21) arranged at a central area of the bottom electrode, and wherein the dielectric spacer (portion of layer 25 that is on the periphery of the lower electrode) is arranged around the projecting portion (fig. 3).

Regarding claim 14, Ochiai teaches (fig. 3) substantially the entire claimed structure of claim 1 above including a ferroelectric capacitor comprising: a first electrode (24) which has a plate portion (peripheral area of 23) and a projecting portion (21), wherein the projecting portion is arranged on a central area of the plate portion; a spacer layer (layer 14 of Basceri) formed on a peripheral area of the first electrode and arranged around the projection portion of the first electrode (refer to fig. 3), a ferroelectric layer (25) formed on the spacer layer (14, Basceri) and on the projecting portion (21); and a second electrode (26) formed on the ferroelectric layer wherein a side surface of the plate portion (peripheral area of 23) of the first electrode, a side surface of the ferroelectric layer (25) and a side surface of the second electrode (26) are aligned (fig. 3).

Regarding claim 16, Ochiai teaches (fig. 3) substantially the entire claimed structure of claim 1 above including a semiconductor substrate (10); a transistor (col. 6, lines 25-42) formed on the semiconductor substrate, the transistor having a source region (15), a drain region (15) and a gate electrode (13); an insulating layer (20) formed on the semiconductor substrate (10) and the switching transistor; a ferroelectric capacitor formed on a top surface of the insulating layer (refer to fig. 3) and plug

electrode (19) connects the source region of the switching transistor to the bottom electrode (24) of the ferroelectric capacitor.

Regarding claim 17, Ochiai teaches substantially the entire claimed structure of claim 16 above including the top surface of the insulating layer (20) is formed substantially flat (fig. 3).

Regarding claim 18, Ochiai teaches substantially the entire claimed structure of claim 16 above including the ferroelectric capacitor is located over the source region (15) of the switching transistor (fig. 3).

3. Claims 19 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ochiai, Basceri in view of Kobayashi US patent No. 6,495,879.

Regarding claim 19, Ochiai teaches (fig. 3) the entire claimed structure of claims 1 and 16 above except explicitly stating a wiring, which connects the source region of the switching transistor to the top electrode of the ferroelectric capacitor.

Kobayashi teaches (figs. 10A-10F) a semiconductor substrate (11); a transistor (col. 9, lines 34-41) formed on the semiconductor substrate (11), the transistor having a source region (source/drain regions 18), and a gate electrode (17); an insulating layer (col. 9, lines 34-41) formed on the semiconductor substrate (11) and a top electrode (15) formed on a ferroelectric layer (14); and a wiring (16) which connects the source region (18) of the transistor to the top electrode (15) of the ferroelectric capacitor (25) (refer to fig. 10F). Furthermore Kobayashi teaches a MOS transistor that is capable of performing as a switching transistor.

Art Unit: 2811

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the transistor connection portion taught by Kobayashi in the structure of Ochiai in order to integrate the ferroelectric capacitor with other portion of the integrated device.

Regarding claim 20, Ochiai teaches substantially the entire claimed structure of claim 19 above including the wiring (16, portion of 16 inside the via) includes a plug portion which extends from the source region (18) of the switching transistor to the top surface of the insulating layer (26) and a wiring portion (portion of 16 that connects to 15) which connects a top of the plug to the top electrode (15) of the ferroelectric capacitor (25).

#### ***Allowable Subject Matter***

4. Claim 4 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

#### ***Reason for indicating allowable subject Matter***

5. The following is a statement of reasons for the indication of allowable subject matter: The prior art of record does not teach or suggest, singularly or in combination at least the limitation of "a top surface of the dielectric layer is substantially coplanar with a top surface of the second region" as recited in claim 4.

#### ***Response to Arguments***

6. Applicant's arguments with respect to claims 1-3, 6-11, 13-14 and 16-20 have been considered but are moot in view of the new ground(s) of rejection.

Art Unit: 2811

***Conclusion***

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Samuel A. Gebremariam whose telephone number is (571) 272-1653. The examiner can normally be reached on 8:00am-4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (571) 272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Art Unit: 2811

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SAG  
June 10, 2005

Steven Loke  
Primary Examiner

